UNITED STATES PATENT AND TRADEMARK OFFICE

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EXAMINER
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ART UNIT	PAPER NUMBER
2122	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

DETAILED ACTION

1.   This action is responsive to the application filed October 30, 2001.

2.   The priority date considered for this application is May 31, 2001, which is the
filing date of the provisional application no. 60/294,913.

3.   Claims 1-19 have been examined.

Drawings

4.   The drawings are objected to because of the following minor informalities:

    a.   Figures 1A and 1B should be designated by a legend such as – Prior Art
– because only that which is old is illustrated. See MPEP § 608.02(g);

    b.   Figures 1A and 1B:

        i.   an arrowhead is missing at the bottom end of the connecting line
between blocks 102, 152 and 104, 154, respectively; and

        ii.   it is not clear why there is a connecting line between the output of
block 104, 154 and the input of block 102, 152 respectively;

    c.   Figure 2:

        i.   Block 206: the terms "empty" and "unknown" should be enclosed
between quotation marks;

        ii.   Block 208: a question mark should be added at the end of the
clause;

        iii.   Block 214: "YES" and "NO" legends are missing at the outputs
of this decision block;

        iv.   Figure 2 on page 3 of 5 should be labeled -- Figure 2A – and the
Figure shown on the next page, i.e., sheet 4 of 5, should be labeled – Figure 2B –
because Figure 2B is a continuation of Figure 2A;

      v.   "YES" and "NO" legends are missing at the outputs of decision blocks 218, 222, 226, 230, 234;

      vi.   destination of output from each of the three boxes labeled "238" should be indicated.

Specification

5.   The specification is objected to because of the following minor informalities:

    a.   the section "Brief Summary of the Invention" is missing;

    <u>Brief Summary of the Invention</u>: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

    b.   The term "complier" at page 1, line 22 is mistyped;

    c.   The term "servelets" at page 1, line 29 is mistyped.

Claim Objection

6.   Claims 2, 6 and 9 are objected to because of the following minor informalities:

    a.   Claims 2 (line 18 of claim) and 6 (line 3 of claim): the terms **empty** and **unknown** should be enclosed between quotation marks;

b.   Claims 2 (lines 31 and 34 of claim) and 9 (lines 5 and 7 of claim): the term **stack** after "mappings to" should be enclosed between quotation marks.

Claim Rejections - 35 USC § 112

7.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8.   Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, claim 3 recites the limitation *using information from preceding instructions to mimic an optimizing compiler,* which is found to be not sufficiently described in the specification so as to convey to one skilled in the art how to write code to perform such a step. First, it is noted that the specification in section 0028, lines 3-5 shows that the preceding translation information is being used rather than *information from preceding instructions* as recited in claim 3. Preceding translation information is different from information from preceding instructions. For art rejection purposes, the limitation is interpreted as *using preceding translation information to mimic an optimizing compiler.* Second, it is unclear what *to mimic an optimizing compiler* explicitly means. The specification does not provide any detailed description of this function.

9.   Claims 4-19 which depend from claim 3 is also rejected under 35 U.S.C. 112, first paragraph for the same reasons.

10.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11.   Claims 2-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

     a.   Lack of antecedent basis:

Claim 2 recites the limitation "said class file" in line 22 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 2 recites the limitation "said mappings" in line 34 of the claim (after "setting"). There is insufficient antecedent basis for this limitation in the claim. The limitation "said mappings" should be changed to – said stack mappings – in order to have proper antecedent basis.

Claims 2 (in line 59 of the claim) and 14 (in line 4 of the claim) recite the limitation "said stack values". There is insufficient antecedent basis for this limitation in the claim.

Claims 4-19 recite the limitation "said compilation procedure" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 9 recites the limitation "said selected actual bytecode instruction" in lines 2-3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 9 recites the limitation "said mappings" (two occurrences) in lines 6-7 of the claim. There is insufficient antecedent basis for this limitation in the claim.

The limitation "said mappings" should be changed to – said stack mappings – in order to have proper antecedent basis.

    b.   Confusing and indefinite:

    Claims 2 (line 25 of the claim) and 8 (line 2 of the claim) recites the limitation "stack maps." It is unclear whether the limitation "stack maps" is the same as the limitation "stack mappings." For art rejection purposes, the limitation "stack maps" is considered equivalent to "stack mappings."

    Claim 3 recites the limitation *to mimic an optimizing compiler*, which is found to be indefinite because one skilled in the art does not know precisely and clearly what and how many optimizing technique(s) to mimic. For art rejection purposes, the limitation *using information from preceding instructions to mimic an optimizing compiler* is interpreted to mean using preceding translation information (e.g., pre-verification step) to give the method the same optimizing result of a compiler such as the one taught by U.S. Patent No. 5,999,731 to Yellin et al. (see instant disclosure, section 0012).

Double Patenting

12.   The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Long*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1993); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F2.d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F2.d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminated disclaimer in compliance with 37 CFR 1.103(c)
1.321(c) may be used to overcome an actual or provisional rejection based on a
nonstatutory double patenting ground provided the conflicting application or patent is
shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a
terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply
with 37 CFR 3.73(b).

13.   Claims 1-19 are provisionally rejected under the judicially created doctrine of
obviousness-type double patenting as being unpatentable over claims 1-29 of
copending Application No. 10/016,794. This is a provisional double patenting
rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the
referenced copending application and would be covered by any patent granted on that
copending application since the referenced copending application and the instant
application are claiming common subject matter or obvious variation thereof, as
shown in the following table(s).

Furthermore, there is no apparent reason why applicant would be prevented
from presenting claims corresponding to those of the instant application in the other
copending application. See *In re Schnelle*, 397 F2.d 350, 158 USPQ 210 (CCPA 1968).
See also MPEP § 804.

Copending Claim 1	Instant claim 1
A computer apparatus suitable for use in the **combined compilation and verification** of platform neutral bytecode instructions resulting in optimized	A computer apparatus suitable for use in the **fast compilation of preverified** platform neutral bytecode instructions resulting in high quality native machine

machine code, comprising:	code, comprising:
a central processing unit (CPU);	a central processing unit (CPU);
a computer memory coupled to said CPU, said computer memory comprised of a computer readable medium;	a computer memory coupled to said CPU, said computer memory comprised of a computer readable medium;
a **compilation-verification** program embodied on said computer readable medium, said **compilation-verification** program comprising:	a **compilation** program embodied on said computer readable medium, said **compilation** program comprising:
a first code segment that receives a **bytecode** listing;	a first code segment that receives a **class file** listing;
a second code segment that **verifies said bytecode listing is free of malicious and improper code and compiles said bytecode** listing into machine code; and	a second code segment that **compiles said class file** listing into machine code; and
a third code segment that interprets and executes said machine code.	a third code segment that interprets and executes said machine code.

Copending claim 7	Instant claim 3
A computer implemented method for **facilitating combined compilation and verification** of platform neutral bytecode instructions resulting in **optimized** machine code, comprising the steps of:	A computer implemented method for **compilation of preverified** platform neutral bytecode instructions resulting in **high quality** native machine code, comprising the steps of:
receiving a class file onto a computer readable medium containing compilation procedure instructions, said class file containing one or more methods containing platform neutral bytecode listings;	receiving a class file onto a computer readable medium containing compilation procedure instructions, said class file containing one or more methods containing platform neutral bytecode listings;
executing said compilation procedure instructions on said bytecode listings, said compilation procedure instructions **also simultaneously verifying** said bytecode listings; and	executing said compilation procedure instructions on said bytecode listings, said compilation procedure instructions **sequentially processing each byte code instruction** of said bytecode listing;

	using information from preceding instructions to mimic an optimizing compiler; and
producing **verified optimized** machine code on said computer readable medium.	producing native machine code on said computer readable medium.

As can be seen from the above tables, all the claims of the instant application are anticipated by those of the copending application. The invention of the instant application, i.e., **method for compilation of preverified platform neutral bytecode instructions,** is not patentably distinct from that of the copending invention since the invention of the copending application is also related to a method for compilation of platform neutral byteceode instructions. The only difference is that the method of the copending application compiles and verifies bytecodes. The same verification step of bytecodes of the copending method has been previously performed by the method of the instant application to ensure that the bytecodes are free of malicious or improper code.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

15. Claims 1 and 3-8 are rejected under 35 U.S.C. 102(a) as being unpatentable over the admitted prior art (APA) of Figures 1A and 1B and of pages 1-6 of applicant's background.

Claim 1

APA discloses at least:

a compilation program embodied on said computer readable medium, said compilation program comprising:

a first code segment that receives a class file listing (see at least Figure 1A, step 102; Figure 1B, step 152; Figure 2, step 202; and associated text);

a second code segment that compiles said class file listing into machine code (see at least sections 0006-0012); *and*

a third code segment that interprets and executes said machine code (see at least Figure 1B, step 154 and associated text; p. 2, line 23-24; p.3, line 14).

The APA of applicant's background does not specifically disclose:

a central processing unit (CPU);

a computer memory coupled to said CPU, said computer memory comprised of a computer readable medium.

However, this hardware support is deemed to be inherent to the APA teaching of a compilation procedure. Without a CPU which executes the instructions of a computer program (e.g., compiler and JAVA™ virtual machine) that is stored on a computer readable medium and loaded onto a random access memory of a computer system, the compilation procedure would be inoperative and would produce no useful, concrete and tangible results.

Claim 3

APA discloses a method for compilation of pre-verified platform neutral bytecode instructions comprising at least:

receiving a class file onto a computer readable medium containing compilation

procedure instructions, said class file containing one or more methods containing platform neutral bytecode listings (see at least Figure 1A, step 102; Figure 1B, step 152; Figure 2, step 202; and associated text; sections 0004-0005);

executing said compilation procedure instructions on said bytecode listings, said compilation procedure instructions sequentially processing each byte code instruction of said bytecode listing (see at least sections 0006-0008);

using information from preceding instructions to mimic an optimizing compiler (see at least section 0012); and

producing native machine code on said computer readable medium (see at least Figure 1B, step 154 and associated text; p. 2, line 23-24; p.3, line 14).

Claim 4

APA further discloses *wherein said compilation procedure said first class to compile* (see at least Figure 1A and associated text; section 0007).

Claim 5

APA further discloses *wherein said compilation procedure selects first method of said first class to compile* (see at least Figure 1A and associated text; section 0007).

Claim 6

APA does not specifically disclose *wherein said compilation procedure creates map storage to store actual mappings and native code addresses and initializes stack mappings to "empty" and addresses to "unknown"*. However, these steps are deemed to be inherent to the teaching of APA (see at least Figure 1A, step 104 and Figure 1B, step 154; and associated text). Without these stored information, optimization would not be possible.

Claim 7

APA does not specifically disclose *wherein said compilation procedure sequentially selects each bytecode instruction in each said method of each said class file.* However, this step is deemed to be inherent to the teaching of APA (see at least Figure 1A, step 102; Figure 1B, step 152; and associated text). As can be seen in steps 102 and 152, each bytecode instruction is analyzed one at a time. Without this looping process that analyzes each instruction and collects information therefrom, optimization would not be possible.

Claim 8

APA further discloses *wherein said compilation procedure detects stack maps for said selected bytecode instruction* (see at least Figure 1A, step 104; Figure 1B, step 154; and associated text).

Allowable Subject Matter

16.   Claim 2 is objected to as containing minor informalities and terms lacking proper antecedent basis but would be allowable if rewritten to correct these deficiencies.

Claims 9-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

It is noted, however, that these claims when taken individually and without including all of the limitations of the base claim and any intervening claims are not allowable.

It is suggested that the aspect of the invention that consists of creating optimized machine code from bytecode in a single sequential pass in which information from preceding instruction translations is used to perform the same

optimizing process of an optimizing compiler without the extensive memory and time requirements be recited in independent claims 1 and 3 to particularly point out and distinctly claim the invention.

Conclusion

17.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

18.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Vu A Nguyen-Ba whose telephone number is (703) 305-0103. The examiner can normally be reached on Tuesday-Friday, 6:00 – 16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on (703) 305-4552. After October 25, 2004, the examiner can be reached at (571) 272-3701 and the examiner's supervisor at (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit 2122

September 2, 2004

ANTONY NGUYEN-BA
PRIMARY EXAMINER